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# Thermal Characterization of Thin Films for MEMS Applications

**by David J. Howe and Brian Morgan**

**ARL-TR-4378** **February 2008**

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**Sensors and Electron Devices Directorate, ARL**

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**14. ABSTRACT**
Thin film dielectrics play an important role in the fabrication and processes involved with microelectromechanical systems (MEMS). Two such dielectrics that are used widely are silicon dioxide ($SiO_2$) and photoresist. As a large portion of these systems use the conduction of heat through $SiO_2$ and photoresist layers, the thermal conductivity of these materials is crucial. In this work, the thermal conductivities of the above mentioned materials were determined using a micro-mesa test structure consisting of the dielectric to be measured sandwiched between two resistive temperature detectors, one acting as a heater. At near room temperature, the thermal conductivity of thin-film PECVD silicon dioxide was determined to be 1.06 $Wm^{-1}K^{-1}$, similar to known bulk values for $SiO_2$. The thermal conductivity of photoresist measured around room temperature was determined to be 0.31 $Wm^{-1}K^{-1}$. Multiple film thicknesses were tested with these structures to account for interface effects.

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# 1. Introduction

Dielectric thin films play a very important role in the development of microelectromechanical systems (MEMS). These dielectric materials often are used as insulating layers in devices, major components in MEMS structures, or even as materials strictly used for fabrication processes in a cleanroom environment. In these applications, heat is often a crucial factor. Whether it be heat transfer through a device to stimulate operation, a device being exposed to certain temperatures during fabrication, or any other manner of heat transfer, these thermal processes are critical to device operation in MEMS. As such, thermal properties of these thin film dielectrics, especially thermal conductivity, are very important parameters to insure proper device operation.

Silicon dioxide and photoresist are two dielectrics that are commonly used in MEMS processes and in a cleanroom environment. $SiO_2$ is often used as an insulating layer between a silicon substrate and device stacks on top of the substrate as well as between conducting layers within the actual device. Photoresist is used in the photolithography process to pattern device layers. It can also be cured using heat and ultraviolet light to be incorporated permanently in devices as an insulator. As these two materials are very commonly used in MEMS development, their thermal properties are of great interest.

At present, thermal conductivity data of silicon dioxide and photoresist at the scale to be studied is very limited (*2, 5*). The majority of known values for these materials are for bulk thicknesses. In comparing known bulk values to those of thinner films, it has been found that a decrease in thermal conductivity results when the size of the test specimen goes from bulk to these thinner films (*2*). Also, process conditions between fabrication environments can vary greatly. For example PECVD $SiO_2$ may be slightly silicon-rich or poor depending on recipe. An increase in silicon content would result in an increase in the thermal conductivity of the dielectric layer. Thus, data from a silicon-rich PECVD would differ from that of a stochiometric PECVD. This lends credence to the uniqueness of process conditions in each laboratory. Therefore, new testing and data has to be collected for these materials specific to the Army Research Laboratory (ARL) cleanroom facility at the scales to be used in MEMS processes.

This work determines the thermal conductivities of thin-film PECVD silicon dioxide and photoresist. Knowing the values of materials processed in the ARL cleanroom will give site-specific values for this information that will take priority over other values determined in the field. These values will directly benefit MEMS development and cleanroom processes for the Army.

## 2. Background/Theory

### 2.1 Current Testing Methods

Presently, there are several methods used in determining thin-film thermal conductivity. The 3ω method developed by Cahill (*4*) is one of the most used methods for thermal characterization. Using this method, the dielectric to be tested is deposited as a thin film on a substrate. A resistive temperature detector (RTD) is then patterned onto the dielectric, as seen in figure 1. This RTD also acts as a heater during testing. The current-conducting pads are connected to an ac source, while the two interior pads are connected to a lock-in amplifier. A current is fed into the device at an angular frequency of ω. The wire is therefore heated at a frequency of 2ω. The lock-in amplifier then records the voltage signal at a frequency of 3ω, since the 2ω frequency in the wire multiplied by the input current at a frequency of ω results in a voltage oscillation across the wire of 3ω. Thus, after a temperature calibration is performed, the thermal conductivity can be obtained using the measurements taken with the lock-in amplifier. This method does not take into account the effects of thermal diffusion through the film into the silicon substrate, which would result in a loss of heat and therefore a variance in thermal conductivity. Most consider the use of an alternating current an "indirect" form of measurement, but a direct form of measurement at steady-state conditions would more accurately mimic application conditions, such as thermoelectric generators.

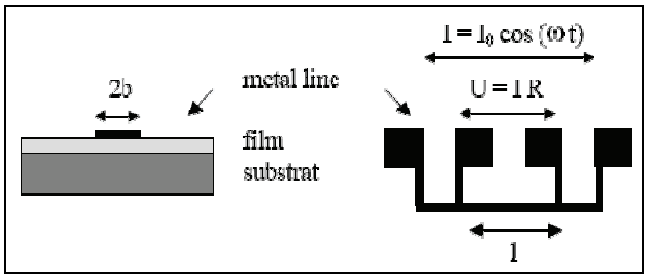


Figure 1. Device layout using the 3ω method.

Another approach to determining thin-film thermal conductivity is the use of finite element analysis (FEA) (*6,7*). This method involves using thermal modeling software in order to determine temperature distributions across the devices to be tested. These simulations can determine the theoretical thermal conductivities of the materials under study. Although these simulations can be quite accurate in predicting the thermal conductivity of bulk structures, software modeling always incorporates a large number of assumptions in development. As variations in the field always exist from the ideal assumptions used in simulation, it is nearly impossible to fully replicate the conditions and structures determined through FEA modeling, particularly for micro-scale applications. Thus, although FEA is a very positive technique to

gain expected data values prior to fabrication and hardware testing, it is limited by the assumptions inherent in the modeling and cannot be used in place of physical experimentation.

The method upon which this work is based involves a micromesa test structure, seen in figure 2 and developed by Kurabayashi, et al. (*1*). The geometry that these mesa structures employ limits the heat path to conduction perpendicular to the surface of the substrate with very little excess heat lost from the sides or top of the structures. This form of testing and measurement constitutes a "direct" measurement of thermal conductivity as DC values are collected from the devices themselves. In this approach, data is collected at "steady state," which is more representative of the application environment for these materials. Thus, the testing conducted on these structures results in data that relies solely on this vertical conductivity, which is ideal for the purposes of this experiment.

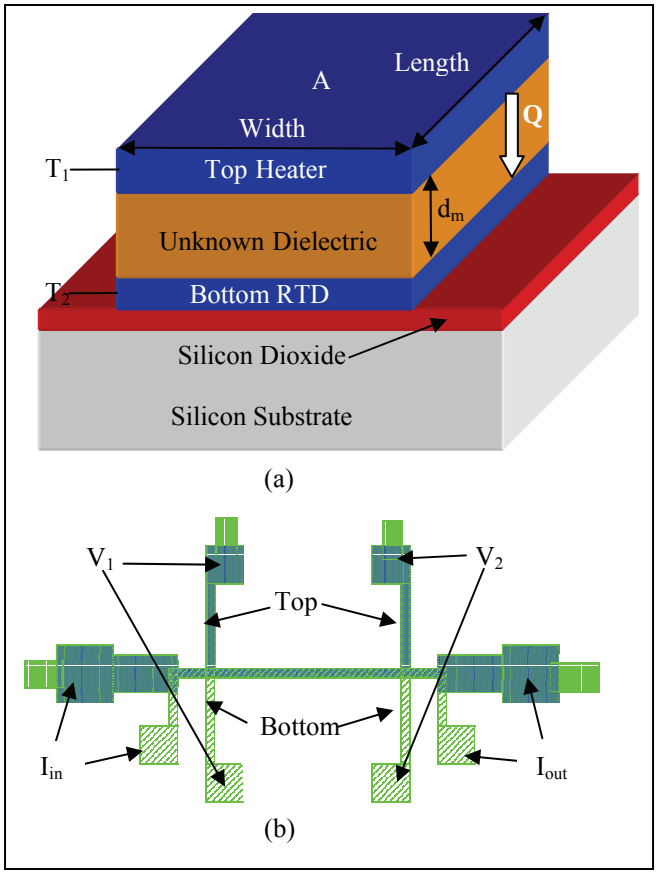


Figure 2. (a) Cross-sectional and (b) top-view geometry of micromesa device structure.

## 2.2 Adapted Testing Method

Continuing from the work of Kurabayashi, et al. (*1*), the dielectric to be measured is fabricated with resistive temperature detectors (RTDs) both above and below it, as seen in figure 2a. A temperature calibration on these RTDs is then performed using a heated chuck in order to attain a change in resistance per unit temperature change, dR/dT, to be used in later calculations. After

this temperature calibration is complete, a 4-point probe testing method is used by first feeding a small fixed current through the bottom RTD. Concurrently, a larger heating current is forced through the top RTD to provide a heat flux (Q seen in figure 2a) through the dielectric layer. Although some heat is generated in driving current through the bottom RTD, it is minimal in comparison to that of the top. Voltage is measured at both RTD's, allowing $R_{final}$ to be calculated. Using the temperature calibration form before, the final temperature of each RTD, $T_{final}$, can be determined:

$$T_{final} = (R_{final} - R_0)\frac{dT}{dR} + T_0 \tag{1}$$

Where $R_0$ is the initial resistance at room temperature, $dT/dR$ is the inverse of the slope of the characteristics for each device calculated from the temperature calibration, and $T_0$ is the base temperature, or room temperature in our work. Using this information, the heat flux, $q$", can also be determined with equation 2, knowing the currents and resistances from 4-point probe testing, as well as the cross-sectional area, $A$, of each device:

$$q'' = \frac{I^2 R}{A} \tag{2}$$

Again, the top RTD current values are used in equation 2 as the heating derived from the bottom RTD will be negligible compared to the top. From the data calculated using equations 1 and 2, the thermal resistance, $R_{th}$, can now be determined:

$$R_{th} = \frac{T_{Top} - T_{Bottom}}{q''} = \frac{d_m}{k_T} + R_{boundary} \tag{3}$$

where $T_{Top}$ is the temperature at the top RTD, $T_{Bottom}$ is the temperature at the bottom RTD, $d_m$ is the thickness of the dielectric layer, and $k_T$ is the thermal conductivity of the dielectric layer. The boundary resistance, $R_{Boundary}$, is expected to be a negligibly small value compared to the thermal resistance and will appear as a DC offset. In practice, multiple step heights of the dielectric layer are fabricated to confirm a small boundary resistance. Finally, the thermal conductivity is determined:

$$k_T = \frac{d_m}{R_{th}} \tag{4}$$

The only necessary parameter that is unknown at this juncture is $d_m$. This can be determined during fabrication using step height measurements taken with a profilometer. Thus, with a simple device structure and direct testing method, the thermal conductivity of a dielectric can be determined through the above-mentioned process.

# 3. Fabrication

## 3.1 Silicon Dioxide Wafer Fabrication

The test devices were fabricated within a cleanroom environment. A thin, 0.5 μm silicon dioxide layer was first deposited using plasma-enhanced chemical vapor deposition (PECVD) onto a polished silicon substrate. This $SiO_2$ layer is used as an electric insulator between silicon substrate and the bottom RTD. On top of this layer, a metal RTD layer was patterned using photolithography. A 100 Å titanium adhesion layer (*3*) was sputtered onto the oxide, followed by an 850 Å platinum layer to act as the RTD. The excess metal was then removed through the use of acetone during the liftoff process. The silicon dioxide layer of interest was then deposited on top of this RTD through the use of PECVD. Three different oxide thicknesses were patterned: 1.18 μm, 1.67 μm, and 2.24 μm. This variation in thicknesses was to account for process variation and confirmation of small $R_{boundary}$. On top of this $SiO_2$ layer, the top metal heater was patterned through the use of photolithography in the same manner as the bottom RTD. A 100 Å titanium adhesion layer and a 1700 Å platinum layer were then sputtered on, before the excess metal was lifted off through the use of acetone once again.

The completed wafers can be seen in figure 3. These wafers contain 6 die with 9 devices per die for each silicon dioxide thickness. On each die, the device lengths are 1 mm, 2 mm, or 4 mm, while the device widths are 50 μm, 100 μm, or 200 μm. This is to ensure as much variation in testing results as possible to elucidate geometrical and/or edge effects.

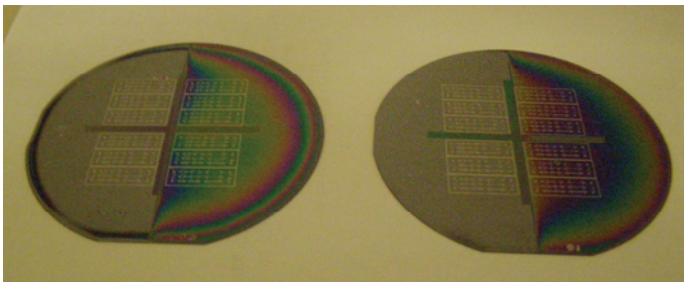

Figure 3. Completed silicon dioxide wafers.

## 3.2 Photoresist Wafer Fabrication

The fabrication of wafers using photoresist as the dielectric was very similar to that of the silicon dioxide wafers described above. A thin, electrically insulating silicon dioxide layer was deposited on the silicon substrate followed by the bottom metal being patterned on using photolithography and liftoff. The photoresist layer to be characterized was then patterned using photolithography and stabilized using a UV curing process at 190 $^{o}$C. The surface of the photoresist was then "roughened" to assist adhesion to the top metal through the use of an $O_2$ plasma descum. The top RTD was then patterned in the same manner as the silicon dioxide

wafers. When these wafers incorporating photoresist were put into acetone for liftoff of the top metal, the acetone was first heated to a temperature of 50 $^{o}$C. This was carried out to prevent the onset of thermal shock in the photoresist layer of the devices during liftoff. As is witnessed in figure 4, placing the wafer directly in room temperature acetone for liftoff causes a thermal shock in the photoresist, resulting in cracking of this layer. Another step that was taken in order to prevent thermal shock was to pattern on a resist for the dielectric layer that was thinner than originally planned. A resist layer of 1.37 μm was used in fabrication rather than the 2.25 μm photoresist layer typically used.

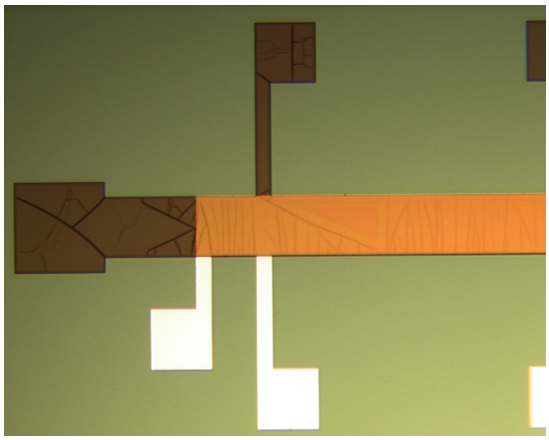

Figure 4. Cracking due to Thermal shock in wafer using photoresist.

## 4. Experimental Setup and Procedure

The substrates fabricated to determine the thermal conductivity of the two unknown dielectrics were tested using a 2-step process, as was briefly described in section 2. The first part of this testing was a temperature calibration of the fabricated devices. To accomplish this, the wafer with the devices to be tested was loaded onto a heated chuck connected to a microscopic probe station. Probes were then connected to a device in the manner shown in figure 2b. For each device, a current and voltage were connected to both the top and bottom RTDs and tested separately. A current of 1 mA was passed through the device while the temperature of the chuck was increased incrementally. The test setup used for this portion of the testing can be seen in figure 5. The voltages were recorded for temperatures in the approximate range from room temperature to 90 $^{o}$C and the resistances for the corresponding voltage and current at each temperature were determined. From this data, temperature versus resistance characteristics were constructed for both top and bottom RTDs of the silicon dioxide and photoresist substrates as well as for each different dielectric thickness present on the wafers. Example data can be viewed

in figure 6, where the resistance increase associated with an increase in temperature of the substrate is very linear, as would be expected.

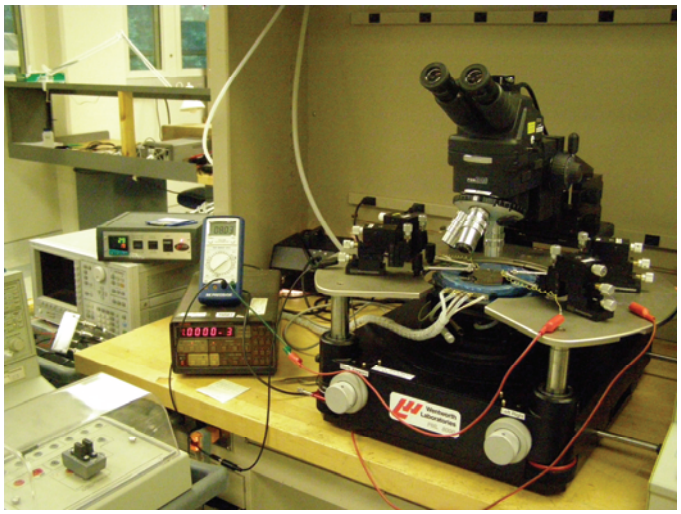

Figure 5. Experimental setup for temperature calibration.

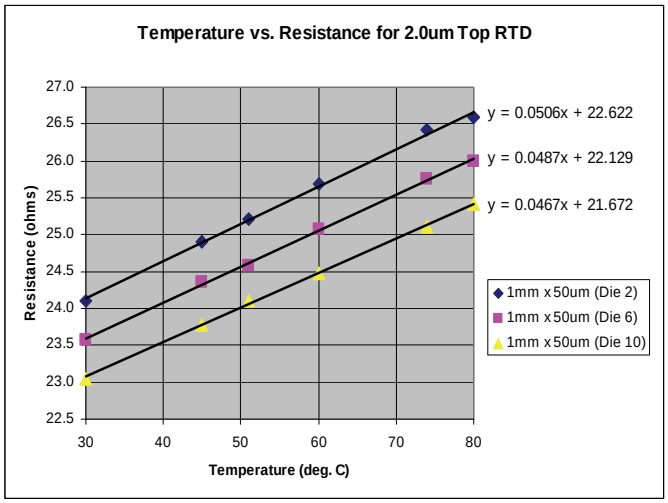


Figure 6. Sample characteristic obtained for 2.0 µm $SiO_2$ top RTD.

The second form of testing conducted on these substrates was the 4-point probe thermal conduction experiment, where a known heat flux was generated in the top resistor and the temperature at the top and bottom RTDs was used in equation 3 to determine the thermal resistance, $R_{th}$. This entailed connecting a current source and voltmeter to both the top heater and bottom RTD of the devices simultaneously. The bottom current was kept at a constant 1 mA, while the current source connected to the top RTD was varied incrementally from 1 mA to 300 mA in order to investigate a range of temperatures. From these two forms of testing, the thermal conductivity of the two materials could be determined incorporating the theory found in section 2.

# 5. Experimental Results

## 5.1. Silicon Dioxide

After testing and calculations were complete, the thermal conductivity of silicon dioxide was determined to be approximately 1.06 $Wm^{-1}K^{-1}$, as seen in figure 7. A similar value was also determined by Kleiner (*2*). Along with the thermal conductivity realization, there were some noteworthy trends that were seen in testing and calculation of results. No significant variation in thermal conductivity was observed between film thicknesses or device geometry. Thus, as expected, thermal conductivity is strictly a material property, regardless of device thickness/shape. This is significant in that the exact thickness of silicon dioxide fabricated on a substrate is often difficult to control. Another point that was realized in our results was the validation of a negligible boundary resistance. Seen in figure 7, the y-intercept of the data is small using the results of just three thicknesses. If more thicknesses were taken, this intercept should approach zero, but as the method we are employing ignores the DC offset, $k_T$ should not be affected regardless (*1*).

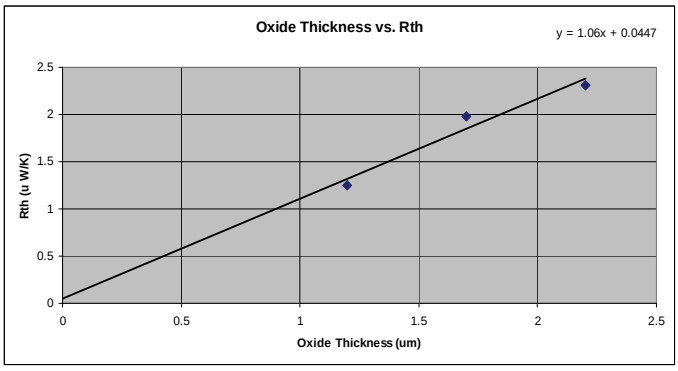


Figure 7. Oxide thickness versus Rth demonstrating negligible boundary resistance.

## 5.2 Photoresist

After testing the devices fabricated using a UV-cured photoresist dielectric layer, the thermal conductivity of this AZ 5214e photoresist was found to be 0.31 $Wm^{-1}K^{-1}$. This value is of the same order of magnitude of 0.19 $Wm^{-1}K^{-1}$, as reported by Hung (*5*). There are many factors that could be attributed to this disparity. One would be in regards to the differing fabrication environments. As process conditions for each laboratory are unique, differing fabrication factors could have attributed to the small discrepancy. For example, depending on bake and curing times, the solvent content of a photoresist layer varies. This could easily have been a major difference in process between our work and that of Hung. This difference would result in a thermal conductivity reflecting upon a higher or lower solvent content present. Another factor would be the low yield of devices for this photoresist characterization. Since adhesion

difficulties were experienced between the top RTD and UV-cured photoresist layer, fewer devices were successfully tested, and at only one film thickness. More confidence in our results would be attained with further testing.

As noted above, the results obtained for the silicon dioxide characterization coincide nicely with those found in literature, which provides validation to the method used.

### 5.3 Error Evaluation

As mentioned previously, the design of the test devices in this work limit heat conduction to the plane perpendicular to the substrate surface, allowing very little heat loss out the sides of the devices. This effect can be demonstrated through a simple calculation (*8*) using:

$$q = hA(T_s - T_f) \tag{5}$$

where $q$ is the heat lost to convection, h is the heat transfer coefficient, A is the surface area under consideration, $T_s$ is the surface temperature, and $T_f$ is the bulk temperature. In carrying out equation 5 for the worst case of our devices, using 15 $Wm^{-2}K^{-1}$ for $h$, 0.4 $mm^2$ for $A$ (surface area of device), and 100 K for $T_s - T_f$, the resultant heat of convection is only 0.6 mW. Comparing this to the actual heat being conducted through the dielectric (typically single-digit Watts), the heat of convection out the top and sides of the devices was deemed negligible.

Although there is negligible error in convective heat loss, there are other small errors inherent in the fabrication and testing methods of these devices. In the fabrication of the test devices on silicon substrates, the exact thickness of each device is not known, as PECVD can vary slightly between runs. Although this is the case, the difference in these thicknesses should be less than 1%. Since the error between deposition runs is so small, it is appropriate to obtain a couple measurements of film thicknesses to use for all devices rather than measuring the thickness of each device individually. A more significant error in the experimental procedure would be that present in the temperature controller for the heated chuck used in the temperature calibration portion of testing. There is an approximately 4% error inherent in the control unit of the chuck that was used, though dR/dT is obtained from the slope of the temperature calibration characteristic.

The final major error in our methods deals with the photoresist characterization exclusively. Although the "cracking" problem seen in figure 4 was resolved, there was still a small adhesion problem that was witnessed, as seen in figure 8. These "ripples" inherent in the top metal RTD are areas where the RTD would not adhere to the photoresist layer. Since the RTD channel is still whole, the devices could be used for testing. However, the ripples would result in erroneous calculations for heat transfer area, as well as interface resistance. There are approximately 6 to 8 of these ripples on the channel of each device, resulting in a small (<5%) error in device area. At the locations of these ripples, the top metal RTD is not in contact with the dielectric. Thus, no heat can be transferred to the metal bridge for measurement purposes at these points. Each of

these locations results in a slight heat loss, and therefore a slight decrease in device area. This error will result in a slight increase in resultant values of thermal conductivity reported. Therefore, there is an estimated 5% error inherent in the $SiO_2$ measurements as well as an approximately 10% error in photoresist measurements.

Figure 8. Example of adhesion problems for photoresist characterization.

## 6. Discussion/Conclusion

This work characterized the thermal conductivity of two dielectric materials commonly used in MEMS processes. This was accomplished through the design and fabrication of test devices on silicon substrates in a cleanroom environment. These devices were then tested in two parts: a temperature calibration, as well as a 4-point probe measurement process to extract data for calculation of thermal conductivity of the test materials. The resultant calculations for the silicon dioxide characterization agree with those found in literature. This lends support to our chosen method of testing. The results determined for the photoresist characterization can also be seen as credible for the ARL cleanroom, given the process conditions and facility-specific procedure that was conducted for fabrication.

The device design and testing method described in this report are valid for any dielectric, allowing for adaptation and use in any application where thermal conductivity would be desired. This method could also be easily modified, using material stacks, for use with conducting materials, such as semiconductors also often used in MEMS processes. This opens up an even broader spectrum for testing and analysis using this method.

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